Appendix M

Title:
Timeslot Assigner Transmit V2.2.1

1 Introduction

1.1 Overview

The Timeslot Assigner Transmit (macro name key: TT_) maps the incoming transmit timeslots (maximal 32 ports x 32 timeslots = 1024 timeslots and for the M256F 28 ports x 24 timeslots = 672 timeslots) to logical channels and provides the channel relevant information to the protocol machine interface. The TSAT provides the timeslot relevant information belonging to this channel to the transmit port interface.

1.2 Features

- coordinates requests of 32 ports [M256F: 28ports] by built-in arbitration
- arbitration priority from low (port n = 0) to high (port n=31)
- channel programming by indirect access through TFPI Slave Interface
- data output FIFO buffering for adjustment of further data processing
- programmable channel assignment per timeslot
- programmable mask per timeslot
- programmable timeslot inhibit flag per timeslot
- remote channelwise loop, one channel at a time (loop RD -> TSAR -> TSAT -> TD)
- remote portwise loop, one port at a time (loop RD --> TSAR --> TSAT --> TD)
- loop supported by a jitter attenuator, consisting of a 512 bit FIFO with slip function
- programmable "TMA1ST flag" (tmafirst flag) to identify the 'first' timeslot for TMA mode channels
- FPI target interface
- performance: SYSCLK up to 70 MHz
- number of gates:
- area:
- power consumption:
- scan path
- RAM (Timeslot Assigner Transmit Parameter Table: TATPT) built in selftest
- RAM (Timeslot Assigner Transmit Data Buffer: TATDB) built in selftest
- RAM (Timeslot Assigner Transmit Fifo: TATFIFO) built in selftest

1.3 System Integration

The TSAT has four interfaces:

- FPI Slave (TFPI) Bus
- parallel REQ/GNT interface to (T)XPI functions (accept incoming timeslot information, provide data to transmit port)
- REQ/GNT interface to PMT functions (provide channel information to processing functions)

- alternate input for remote loop (for one channel or port at a time)

The TSAT receives the port and time slot information from the (T)XPI block. The incoming timeslot is mapped to logic channel information and provided to the protocol machine. Finally the channel relevant data from the protocol machine and mask bit field information is provided to the transmit port interface. Additionally this data can be selected for one single channel or port from the remote loop interface. The mapping information is programmed to the TSAT via the FPI Slave interface.

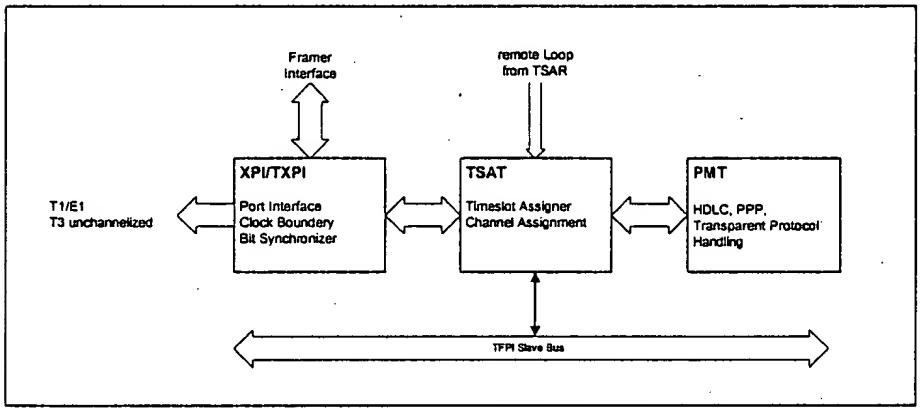


Figure 1:
System integration

1.4 Known Restrictions

1) necessary minimum SYSCLK to serve 32 ports at E1 data rate (32 timeslots), without regarding synchronization losses

   one access request per timeslot; i.e. 2.048Mbit x 32 ports / 8bits/timeslot = 8 Mbyte/s and 4 clock cycles for processing (arbitration, mapping, data transfer) 33MHz SYSCLK would be sufficient.

   in m256f application, i.e T1 1.544Mbit x 28ports / 8bits/timeslot = 5.4 Mbyte/s and 4 clock cycles for processing, the minimum frequency for SYSCLK = 22 MHz.

2) priority and waitstates for indirect read/write access from the FPI slave interface to the TSATPT RAM.

   For operation with maximum data rate, data processing takes every forth clock cycle access to the TSATPT RAM. Else the TFPI slave interface has access to the

TATPT. Thus an indirect write access can be delayed 1 clock cycle for write and 3 clock cycles for read.

3) restrictions regarding the remote loop:

a) Channelwise loop: same port for receive and transmit direction, same number of timeslots activated (inhibit bit = 0), identical mask bit field for all timeslots that are activated activated

b) Portwise loop: same port for receive and transmit direction, only one channel is supported which comprises all timeslots, inhibit bits are not allowed, identical mask bit field for all timeslots

4) timeslot to channel assignment programmed in the parameter table for unchannelized mode .

for unchannelized mode all timeslots of a port have to be assigned to one channel,. valid timeslots are timeslot 0 to 23.

2 Functional Description

2.1 Block Diagram

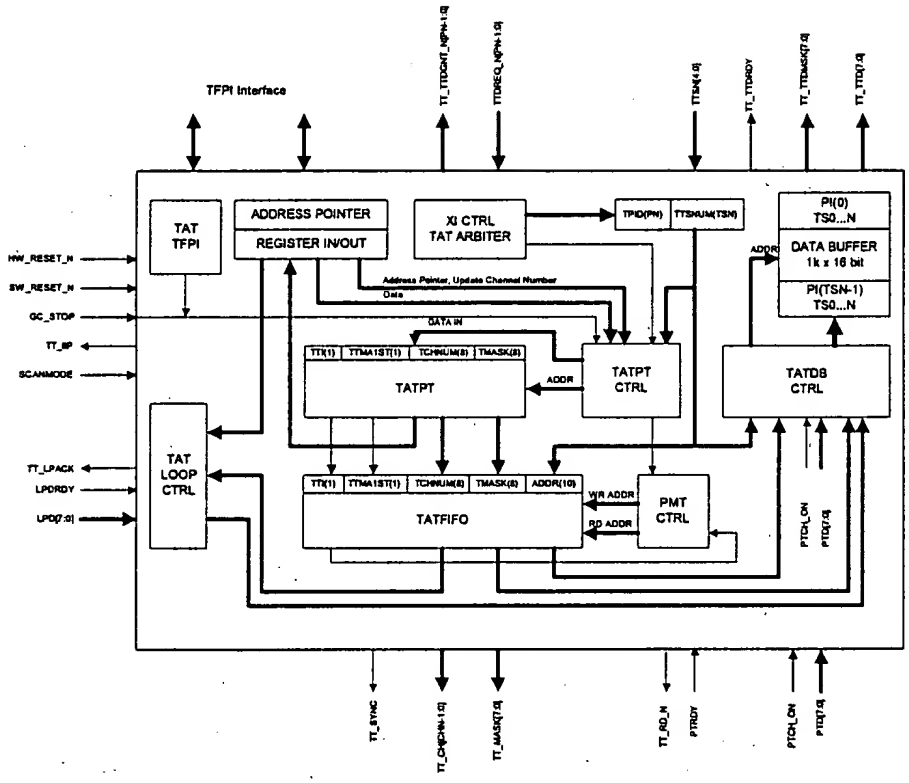


Figure 2.1:
TSAT Block Diagramm

2.2 Normal Operation Description / Reset

With an active reset (HW_RESET_N or SW_RESET_N) all registers are set to their benign state and the TSATFIFO is reset to empty (there is no difference between HW and SW reset). After the reset signal has become inactive, the TSATPT RAM (TSAT Parameter Table) starts its self initialization procedure, resetting the RAM values to TI = '1' (inhibit timeslot), TMA1ST = '0' (no TMA sync timeslot), CHNUM=00_H (channel number 0) and MASK = 00_H (all bits masked). An initialisation procedure is also done for the buffer RAM to transmit port interface, setting the RAM values of data to TTD = FF_H and mask bits to TDMSK = 00_H (all bits masked)

During this initialization period the TSAT is hold in stop mode. The TSAT is inaccessible from all interfaces and doesn't generate any request itself. The active self init period is indicated by output TT_IIP = '1', which becomes '0', when both RAMs (TATPT and buffer RAM) have been initialized.

For fast initialization of the TATPT RAM an input GC_STOP is still asserted (reset value) and keeps the TSAT in stop mode. In stop mode the control logic assigns the TATPT access exclusively to the TFPI interface and normal operation to this RAM is suspended. Thus the initial programming of the TATPT can be achieved very fast since it is not interleaved by normal operation accesses. A request from the (T)XPI will be processed as in normal operation mode, but setting the data to TT_TTD = FF_H and mask to TT_TTMSK = 00_H (all bits masked). The TATPT is programmed now by writing to the two TSAT indirect access registers. The TATPT address corresponds to the time slot number and port number.

In normal operation mode (GC_STOP='0') TFPI re-programming requests to TSATPT are handled by the control logic as ordinary requests for access. Therefore they can be delayed up to 1 clock cycle for write until the access is granted. For read cyles valid data is delayed 2 additional clock cycles because the access to the TATPT is pipelined. Before reprogramming a channel to timeslot mapping configuration the corresponding channel must be turned off, in order to avoid intermediate TATPT states for timeslots of that channel. The TATPT contains the following entries per time slot (address):

TATPT.TI (inhibit transmit time slot)

TATPT.TTMA1ST (flag to be used by PMT in TMA mode)

TATPT.TCHNUM[7:0] (channel number for that timeslot)

TATPT.TMASK[7:0] (mask bits for that timeslot)

After deasserting the GC_STOP input signal, the TSAT is in normal operation mode. The arbiter now accepts requests from (T)XPI signals TTDREQ_N and grants the time slot number bus TTSN to the selected initiator by asserting the corresponding grant signal TT_TTDGNT_N. After deasserting of the corresponding TTDREQ_N signal (marks valid

information on the bus) TTSN is sampled for internal processing. When the TT_TTDRDY line is active TSAT will provide 8 bit data TT_TTD and 8 bit mask field TT_TTDMSK.

To achieve high data throughput, data processing from XPI to PMT is pipeline oriented. The requests for data processing from (T)XPI are provided from a data buffer RAM with one entry for every timeslot of each port. After processing the read transaction to PMT the RAM location for this timeslot is updated.

The following information is received from the (T)XPI:

requests for data processing from the (T)XPI : TTDREQ_N[PN-1:0]

timeslot number bus of grantet (T)XPI : TTSN[4:0]

The following information is delivered to the (T)XPI:

grant signal to select one of the (T)XPI: TT_TTDGNT_N[PN-1:0]

transmit timeslot data for granted (T)XPI: TT_TTD[7:0]

transmit mask bit field for granted (T)XPI: TT_TTMSK[7:0]

finished data transaction for one of the (T)XPI: TT_TTDRDY

The timeslot number, which is received on bus TTSN is combined with the port ID, that the arbiter generates from the corresponding request line TTDREQ_N. The concatenation of timeslot number and port id point to a location in the TATPT. The corresponding contents are read and written into the TATFIFO. A transfer to the PMT is started by TSAT by activating the request line TT_RD_N. In the same cycle the channel number and the mask lines are activated. For the first active timeslot of each logical channel in TMA mode, the TSAT activates the TT_SYNC line. This TMA1ST info flag is used in the protocol machine transmit for synchronisation purposes to indicate the first timeslot in a frame, which is assigned to a multi-timeslot TMA channel. It must also be set for a single timeslot TMA channel. If TI (timeslot inhibit) is set, no request to the PMT will be generated for this timeslot. Nevertheless the timeslot entry in the TATDB for the (T)XPI request is updated, setting the data to TTD = FF_H and mask to TTMSK = 00_H (all bits masked).

The data transaction is finished by PMT when the PTRDY line is active. Data and channel status information from PMT are sampled and the timeslot entry of the corresponding channel in TATDB is updated. If the channel status signal from the PMT indicate the off status, the entry in the TATDB for the mask is set to TTMSK = 00_H, and for TTD is set to FF_H.

The following information is delivered to the PMT:

the assigned channel number: TT_CH[7:0]

the programmed mask for that timeslot: TT_MASK[7:0]
the TMA1ST info flag: TT_SYNC

The following information is received from the PMT:
the transmit data from the PMT: PTD[7:0]
"channel on" status of the PMT: PTCH_ON

2.3 Remote Loop

A basic channelwise or portwise remote loop is available from the TSAR to the TSAT. The payload of one (and only one) logical channel or port is mirrored from the receive part to the transmit part of the looped port. In SCM mode, the framing bits, CRC and spare bits are not looped. They are provided by the M256F framer and the facility data link controller. The channel number or port ID is programmed in the configuration register 2 CONF2. The loop is activated by setting the corresponding loop command bit located in CONF2. Receive timeslots of that channel or port matching the programmed channel number or port ID are written to the TSAR loop FIFO (64 x 1 byte) which is implemented as a circularly organized memory controlled by a read pointer and a write pointer. The loop FIFO acts as a jitter attenuator which compensates the clock jitter between receive and transmit clock.

As soon as data is available on the remote loop interface, the LPDRDY signal is activated by the TSAR. The data transfer will be processed with transmit timeslots of the channel or port matching the programmed channel number or port ID. For the looped channel or port no request to the PMT will be generated. The data coming from TSAR and mask information read from the TATFIFO is written into TATDB at the RAM location for the timeslot requested by TXPI. The loop is turned off by resetting the loop command bit. The LPDRDY signal is then deactivated, and the loop FIFO will be reset to empty.

Only one loop command bit, either for channel or port loop, should be set at a time. Generally, the port number or channel number has to be programmed first before setting the portwise or channelwise loop command bit.

In case of a channel loop, the channel characteristics in receive and transmit direction must be identical. The numbers of active receive and transmit timeslots of the looped channel must be identical. The mask bit fields in the active timeslots must be identical.

In case of a port loop, only one channel is allowed which comprises all timeslots. Inhibit bits for the looped port are not allowed.

The data transfer for the looped channel or port to the PMR is not affected.

Slip Function

After activating the loop, 32 receive data bytes are written to the loop FIFO until the LPDRDY signal is asserted by TSAR. During this loop FIFO initialization phase,

LPDRDY is still deactivated. The timeslot entry in the TATDB is updated with TTD=FF_H and TTMSK=00_H (all bits masked). When LPDRDY is asserted by TSAR, TSAT starts reading the transmit data from the loop FIFO. The initial distance between the FIFO read pointer (RP) and the write pointer (WP) is 32 bytes. Due to a RCLK/TCLK clock jitter the RP may move towards WP. In case the distance between RP and WP is equal plus/ minus 1 byte a slip of the read pointer will occur. Provided RP is faster than WP a positive slip occurs (the previously received 31 bytes are read out twice). In case RP is slower than WP a negative slip occurs (the next 31 received bytes are skipped). The slip condition is checked with each access to the loop FIFO.

3 Macro Interfaces and Signal Description

All signals are active high until otherwise specified. Active low signals are designated by "_N" appended to their names. To make the design as re-usable as possible, a bus signal whose width is application dependent is specified with one of the following parameters:

Parameter name	Bus Type	Typical Value (Bits) M256F
PN	max. port number bus	5
TSN	max. timeslot number bus	5
CHN	max. channel number bus	8
PAD	port address	5
DB	data bus width	32
AB	address bus witdh	30

3.1 Signal Description

3.1.1 Global Signals

Signal Name	Direction	Type	Tsu/ Thld Td	meaning/comment special characteristics
SYSCLK	i			internal system clock
HW_RESET_N SW_RESET_N	i i			general SW and HW Reset
SCANMODE	i			SCAN Test mode
GC_STOP	i			external init keeps TSAT in stop mode, exclusive access to TATPT RAM from TFPI
TT_IIP	o			TSAT initialization in progress following HW reset. TSAT is not availble when this signal is asserted. This signal will remain high for several clocks following release of TSAT reset(s).

3.1.2 Transmit Port Interface

The XPI(TXPI) interface consists of the following signals

Signal Name	Direction	Type	Tsu/ Thld Td	meaning/comment special characteristics
TTDREQ_N[PN-1:0]	i			request from transmit port n=index for servicing/ reading 8 bit data and 8 bit mask field
TTSN[TSN-1:0]	i			time slot bus containing the time slot number for the data TT_TTD and mask TT_TTDMSK (valid time slot numbers are 0 to 23 for T1, 0 to 31 for E1 **and for unchannelized mode all timeslots of a port have to be assigned to one channel**
TT_TTDGNT_N[PN-1:0]	o			ttsn bus is granted to transmit port n=index
TT_TTDRDY	o			TSAT has finished data transfer in current clock cycle
TT_TTD[7:0] TT_TTDMSK[7:0]	o			data bus containing 8 bit time slot data and 8 bit mask bit field

Description of the (T)XPI interface protocol:

As soon as any port TXPI[n] needs 8 bit data for transmit, it asserts the request signal TTDREQ_N to the arbiter part of the TSAT, in order to request service. The arbiter then grants by activating the respective grant signal TT_TTDGNT_N one port access to the bus TTSN (transmit time slot number). TTDREQ_N is deasserted to indicate valid data in the next clock cycle on the bus TTSN. TT_TTDRDY is activated to indicate that the current data transfer has finished in the current clock cycle and valid data on the busses TT_TTD and TT_TTDMSK is available.

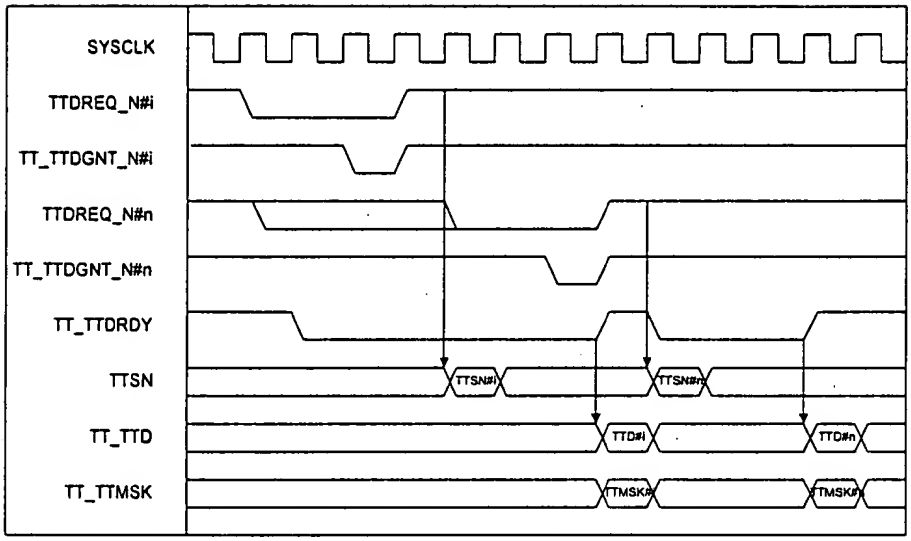


Figure 3.1.2:
Data Transfer from XPI (TXPI) to TSAT

3.1.3 Protocol Machine Transmit Interface

The PMR interface consists of the following signals:

Signal Name	Direction	Type	Tsu/Thld Td	meaning/comment special characteristics
TT_RD_N	o			request for servicing/ reading data
TT_CH[CHN-1:0]	o			logical channel number
TT_MASK[7:0]	o			8 bit mask field to enable single bits of TSA data
TT_SYNC	o			logical channel synchronization line in TMA mode
PTRDY	i			PMT finished data transaction
PTD[7:0]	i			8 bit data from read transaction
PTCH_ON	i			"channel on" status signal from PMT '0' -> channel is not active '1' -> channel is actice

Description of PMT interface protocol:

Whenever data in the TATFIFO is available a transfer is started by TSAT asserting the signal TT_RD_N. In the same cycle channel number and mask information is provided. For the first active timeslot of each logical channel in TMA mode, the TSAT also actives the TT_SYNC line. The information is hold stable until PMT finished data transaction by activating the line PTRDY with valid data on the bus PTD and channel active indication by signal PTCH_ON.

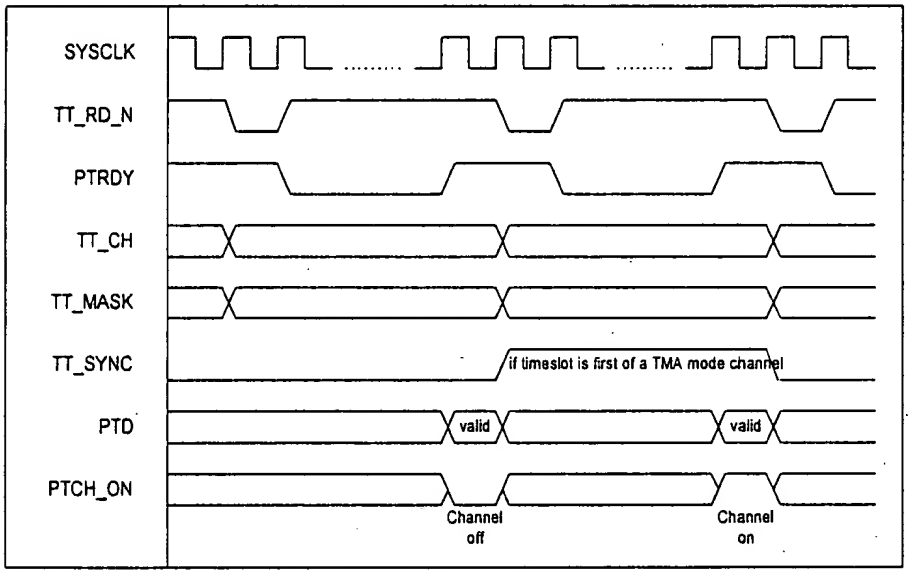


Figure 3.2:
Data transfer from TSAT to PMT

3.1.4 TSA Receive Interface (for remote loop)

TheTSA reveive interface consists of the following signals

Signal Name	Direction	Type	Tsu/ Thld Td	meaning/comment special characteristics
TT_LPACK	o			acknowledge from TSAT data has been read
LPD[7:0]	i			8 bit timeslot data of channel or port which is in remote loop operation
LPDRDY	i			indicates valid data and mask bit field

Description of TSA receive interface protocol:

The remote loop is activated by programming channel number or port ID and the corresponding loop bit CRLP or RLP set in the global mode register. As soon as the loop fifo in TSAR has filled up, LPDRDY signal is asserted. The loop data LPD is read and written by TT_LPACK signal. The remote loop is deactived by resetting the corresponding loop bit.

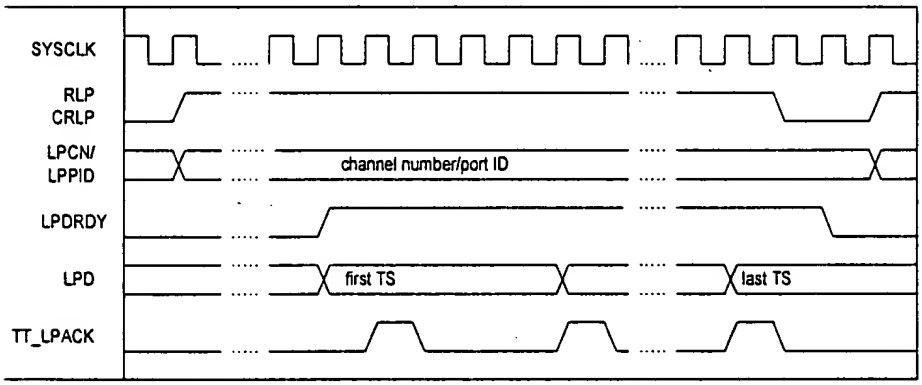


Figure 3.3:
Data transfer on the loop interface

3.1.5 FPI Slave Interface

In the following sections, "Flexible Peripheral Interconnect (FPI) Bus compliant" means that the specified bus uses a subset of the FPI features and satisfies the basic address and data cycle. Not all FPI signals are implemented because default values are sufficient for the application i.e. they can be coded as constants in the hardware. Refer to the FPI bus specification and FPI + Target Template Bus for details of the complete bus.

The TFPI interface consists of the following signals

Signal Name	Direction	Type	Tsu/ Thld Td	meaning/comment special characteristics
TFPI_RD_N	i			Read control input
TPFI_WR_N	i			Write control input
TFPI_A[AB-1:2]	i			Address input
TFPI_D[DB-1:0]	i			Data input
TFPI_RDY	i			Ready input
VG_TFPI_SEL_N	i			(Macro) select input (broadcast programming virtual global register)
TFPI_SEL_N	i			(Macro) select input (macro specific programming)
TT_TFPI_D[DB-1:0]	o			Data output
TT_TFPI_D_EN	o			Data enable (active high)
TT_TFPI_RDY	o			Ready output
TT_TFPI_RDY_EN	o			Ready enable

4 Register Description

4.1 Register Overview

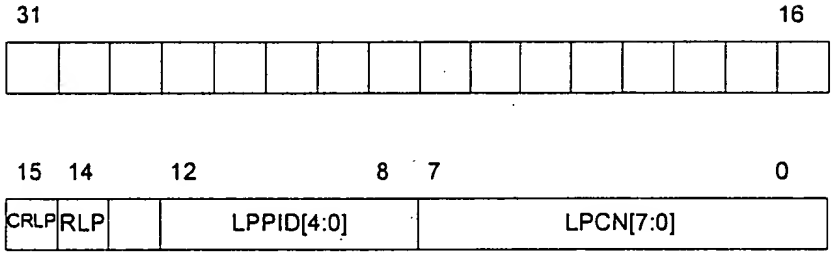
Register Overview Table : TSAT V2.1

Register ID	Access	Absolute Address cs_n & a(7:2)	Reset Value	Comment
CONF2	R/W	44_H	00000000_H	(virtual global) configuration register 2
TSAIA	R/W	70_H	00000000_H	(macro specific) timeslot assignment indirect access register
TSAD	R/W	74_H	02000000_H	(macro specific) timeslot assignment data register
TAC	R/W	58_H	00000000_H	(virtual global) test command register
TD	R/W	$5C_H$	00000000_H	t(virtual global) test data register

4.2 Detailed Register Description

4.2.1 (Virtual Global) Configuration Register 2 (CONF2)

Access : read/write
Address : 00000044_H
Reset Value : 00000000_H



Note: This register is common for TSAT and other macros. The macro TSAT just collect those data bits from the written dword (see above), that are relevant for macro TSAT. With a read access to this register, the macro TSAT drive only a value for the relevant bits. All other bits are set to '0'.

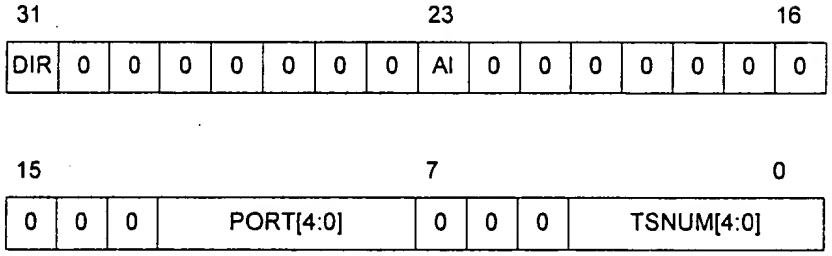
LPCN[7:0]:	Channel selection for channelwise remote loop
LPPID[4:0]:	Port selection for portwise remote loop
CRLP:	'1'--> channelwise remote loop on channel selected by LPCN[7:0]
RLP:	'1' --> portwise remote loop on port selected by LPPID[4:0]

4.2.2 Timeslot Assignment Indirect Access Register (TSAIA)

Access : read / write

Address : 00000070_H

Reset Value : 00000000_H



Address:

This register specifies the base address for access to the TATPT (TSAT parameter table RAM). The address is composed of timeslot number and port id. The address bit field TSNUM[4:0] corresponds to the timeslot number of port which is selected by the address bit field PORT[4:0].

TSNUM[4:0]	timeslot number which is affected by access (T1 = 0..23, E1 = 0..31)
PORT[4:0]	port number which is affected by access (port 0..31)

DIR: transmit/receive direction

1--> Timeslot Assigner Transmit

0--> Timeslot Assigner Receive

AI: auto increment mode

If set when writing a start address to the address pointer, the TSNUM bit field of the address will be automatically incremented (and wrapped at the maximum value x1F) after each read or write access to the data register.This simplifies the transfer of data blocks because the address register for a certain port has to be written only once at the beginning of a data transfer.

Read access to TSAIA

On read access to TSAIA TSAT responds, when DIR is set to '1' (which needs a write access first in order to set DIR). When DIR is set to '0' the TSAR should respond. The macro, which is not accessed, should respond with all '0'.

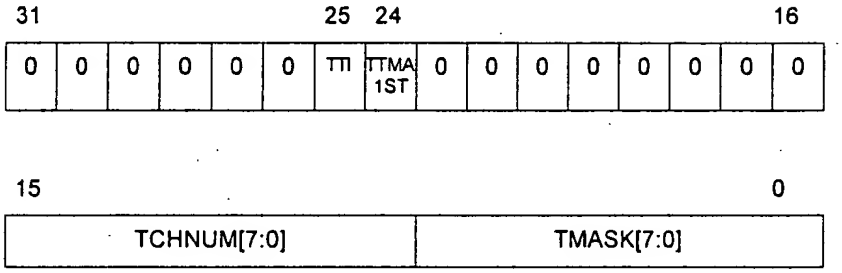
In case having used the autoincrement mechanism before, the returned value should be the actual address, i.e. the autoincremented timeslot number.

4.2.3 Timeslot Assignment Data Register (TSAD)

Access : read/write

Address : 00000074_H

Reset Value : 02000000_H



The data register is a port into the TATPT RAM for read and write access. The RAM address is specified by the address bit field in the timeslot assignment indirect access register. The TATPT RAM is initialized following hw_reset_n.

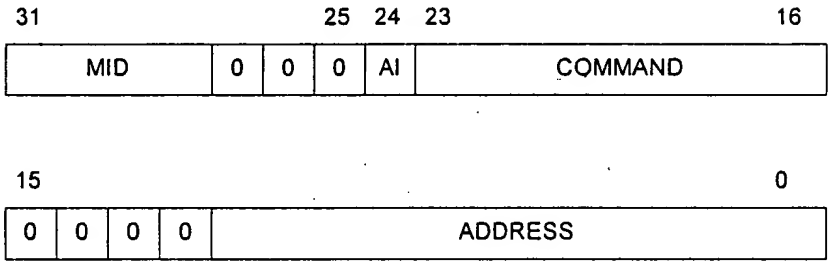
TMASK[7:0]	transmit mask bit field for bit rate adaption, mask bit = '1' bit is enabled, mask bit = '0' bit set to tristate (reset value = 00_H)
TCHNUM[7:0]	transmit channel number, maps the corresponding timeslot to this logical channel (reset value = 00_H)
TTMA1ST	transmit TMA first (for TMA synchronisation purpose), TMA = '1' indicates first timeslot in a logical TMA channel (reset value = '0')
TTI	transmit timeslot inhibit, TTI = '1' no request to the protocol machine for this timeslot, timeslot is set to tristate (reset value = '1')

4.2.4 (Virtual Global) Test Command Register (TAC)

Access : read / write

Address : 00000058_H

Reset Value : 00000000_H



Refer to the Implementation Specification M256F for details to the TAC register.

MID:	Macro ID Code (**TSAT: "0111"**)
AI:	auto increment function
ADDRESS:	internal address
CMD:	command (select of RAM or register)

CMD:

Specifies the access to memory block or register being addressed. Defined command types are :

00000001 : TATPT testmode read (TSAT parameter table RAM)

10000001 : TATPT testmode write

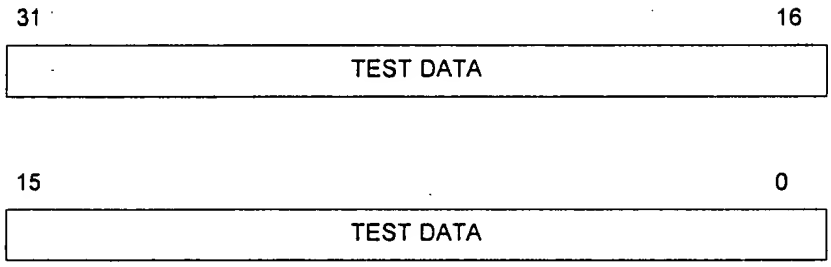
00000010 : TATDB testmode read (TSAT timeslot data buffer RAM)

10000010 : TATDB testmode write (TSAT timeslot data buffer RAM)

On read access to TAC the macro which is selected via MID should respond to this access. All other macros should respond with all '0'.

4.2.5 Test Data Register (TD)

Access ; read/write
Address : $0000005C_H$
Reset Value : 00000000_H



Refer to the Implementation Specification M256F for details to the TD register.

The TD register is a port into theTSAT RAMs TATPT (TSAT parameter table RAM) and TATDB (TSAT data buffer RAM) for read and write access. The selet of RAM and access type is specified by the command bit field in the register TAC. The RAM address itself is specified by the address bit field in the register TAC.

TATPT: TSA transmit parameter table RAM

TEST DATA[7:0]: transmit mask bit field
TEST DATA[15:8]: transmit channel number
TEST DATA[16]: transmit TMA1ST flag
TEST DATA[17]: transmit timeslot inhibit
TEST DATA[31:18]: '0'

TATDB: TSA transmit data buffer RAM

TEST DATA[7:0]: transmit data to XPI (TT_TTD)
TEST DATA[15:8] transmit mask to XP (TT_TTMSK)
TEST DATA[31:16]: '0'

5 Functional Test Specification (Macrolevel)

(use Checklist C06 "Function Checklist - Comparison of Specification vs. Circuit"
http://www.hl.siemens.de/lognet/hl_ta/dhb/f.htm)